REMARKS

This Amendment responds to the Final Office Action mailed November 21, 2006, in the above-identified application. The Amendment does not raise new issues or require extensive consideration. Accordingly, entry of the Amendment and allowance of the application are respectfully requested.

Claims 1-3, 5-8, 11-15, 17-19 and 22-30 are pending in the application. By this Amendment, independent claims 1 and 17 have been amended. No new matter has been added.

The Examiner has rejected claims 1-3, 5-8, 11-15, 17-19 and 22-30 under 35 U.S.C. §102(b) as anticipated by Parthasarathy (US 6,671,799). The rejection is respectfully traversed in view of the amended claims.

Parthasarathy discloses a system and method for dynamically sizing hardware loops and executing nested loops in a digital signal processor. The disclosed apparatus includes N pairs of loop start registers and loop end registers, each loop start register storing a loop start address and each loop end register storing a loop end address, and N comparators, each of the N comparators associated with one of the N pairs of loop start registers and loop end registers. Each of the N comparators compares a selected one of a first loop start address and a first loop end address to a fetch program counter value to detect one of a loop start hit and a loop end hit (col. 2, lines 14-25). The fetch stage compares the fetch PC value to the contents of all three loop addresses corresponding to the three loops (col. 5, lines 31-33). The loop start/end detection circuit is shown in Fig. 3 of Parthasarathy. Output results of comparators 321-323 are provided to priority match circuitry 305, which resolves instances of multiple hits according to the convention that loops are always fully nested (col. 7, lines 31-38).

Parthasarathy does not disclose or suggest "selecting, in a single loop top selector, only the loop top address of the current entry from the loop top addresses in the register file, comparing, in a single loop top comparator, a current instruction address only with the selected loop top address to determine a loop top match, selecting, in a single loop bottom selector, only the loop bottom address of the current entry from the loop bottom addresses in the register file, and comparing, in a single loop bottom comparator, the current instruction address only with the selected loop bottom address to determine a loop bottom match", as required by amended claim 1. Parthasarathy does not

disclose the concept of a current entry in the register file or of selecting and comparing only the parameters of the current entry. Instead, Parthasarathy compares the loop top or loop bottom for all of the loops to a fetch program counter, as shown in Fig. 3. This operation is necessary because Parthasarathy operates "according to the convention that loops are always fully nested" (col. 7, lines 37-38). By contrast, nested program loops can be handled according to the present invention by providing two loop buffers, each with a register file as shown in Fig. 3 (page 8, lines 21-25 of the specification). Parthasarathy does not disclose or suggest selecting and comparing only the loop top address of the current entry and selecting and comparing only the loop bottom address of the current entry, as required by amended claim 1. For these reasons, amended claim 1 is clearly and patentably distinguished over Parthasarathy, and withdrawal of the rejection is respectfully requested.

Claims 2, 3, 5-8 and 11-15 depend from claim 1 and are patentable over Parthasarathy for at least the same reasons as amended claim 1.

Regarding amended claim 17, Parthasarathy does not disclose or suggest "a single loop top selector for selecting only the loop top address of the current entry from the loop top addresses in the register file, a single loop top comparator for comparing a current instruction address only with the selected loop top address to determine a loop top match, a single loop bottom selector for selecting only the loop bottom address of the current entry from the loop bottom addresses in the register file, and a single loop bottom comparator for comparing the current instruction address only with the selected loop bottom address to determine a loop bottom match", as required by amended claim 17. Parthasarathy contains no disclosure of a current entry in the register file or of selecting and comparing only the parameters of the current entry. Instead, Parthasarathy discloses comparators for comparing the loop top or loop bottom for all of the loops to the program fetch counter. For these reasons and for the reasons discussed above in connection with claim 1, amended claim 17 is clearly and patentably distinguished over Parthasarathy. Accordingly, withdrawal of the rejection is respectfully requested.

Claims 18, 19 and 22-30 depend from claim 17 and are patentable over Parthasarathy for at least the same reasons as claims 1 and 17.

Based upon the above discussion, entry of the Amendment and allowance of claims 1-3, 5-8, 11-15, 17-19 and 22-30 are respectfully requested.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

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Respectfully submitted,

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